Project Plan

| Team name: |  |
| --- | --- |
| Members name: | Peter Luick, Yizheng Yu |
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Deadline and grading

|  | Peter Exam Schedule | Yizheng Exam Schedule | CS552 Assignment Due Date |
| --- | --- | --- | --- |
| 20,22-Feb | 17-Feb | HW 3  28-Feb |
|  | 10-Mar  \*(4 days bef Demo 1)  13-Mar  \*(1 day bef Demo 1) | HW 4  30-Mar |
| 3,12-Apr | 3 ~7-Apr(TBD)  14-Apr | HW 5  13-Apr  \*(same date as Project Cache FSM) |
| 7,9,10,11-May | 5, 7, 8-May  10-May  \*(same date Final report) | HW 6  04-May  \*(3 days bef Final demo) |

Design Plan

We plan to partition the work by units. Each person is responsible for some units of the design. We will have one schematic diagram. We will follow the names of modules specified in the schematic diagram so that if any one of us needs to use the other’s module, the port names will be consistent and thus avoid any unnecessary correction.

| Milestone | Peter’s role | Yizheng’s role |
| --- | --- | --- |
| Demo1 (14%)  Unpipelined Design | Control Unit  Register files | Instruction memory  Data memory |
| Demo2 (30%)  Pipelined Design |  |  |
| Cache Demo (15%) |  |  |
| Final Demo (30%) |  |  |
| Final Report( |  |  |

Test Plan

For testing, in addition to the given testing suite, we plan to write our own testbench. Each one will only write testbench for the modules that he designed.